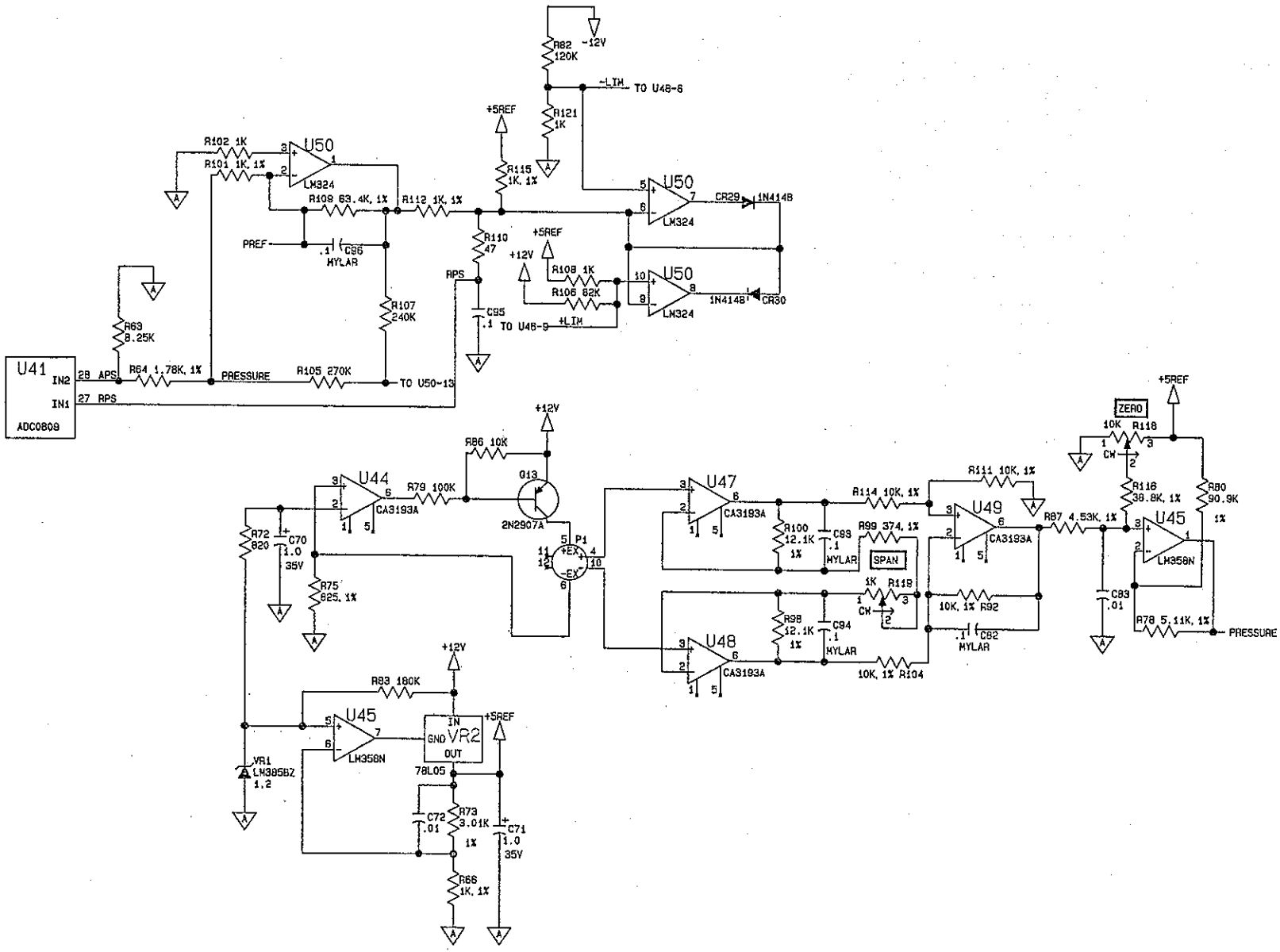

Figure 3-16. Pressure Channel

- RPS. The relative pressure signal (RPS), used by the CPU to detect pulse, originates at error amplifier U50 pin 1. This error amplifier output at pin 1 drives input channel 1 of the A/D converter (U41 pin 27) via a voltage divider/ level shifting network R112 and R115 and isolating resistor R110. U50 (pins 5, 6, and 7) and U50 (pins 8, 9, and 10) are an active clamp to prevent the relative pressure signal from exceeding the input voltage limits of the A/D. Voltage divider R121 and R82 provide a negative reference voltage at U50 pin 5 (and also U46 pin 6) and voltage divider R106 and R108 provide a positive reference voltage at U50 pin 10 (and also U46 pin 9). If the relative pressure signal exceeds the negative reference (more negative), U50 pin 7 will go positive, forward biasing CR29, clamping the relative pressure signal. If the relative pressure signal exceeds the positive reference, U50 pin 8 will go negative, forward biasing CR30 and clamping the signal.

3.6 USER INTERFACE (figures 3-17A and 3-17B)

The user interface comprises U40, speaker LS1, and the user mode selector, pressure selector logic, and DISPLAY TEST switch.

U40 is a three port device. It is selected by USER- from the I/O address decoder. Further decoding of the registers is done with BA0 and BA1.

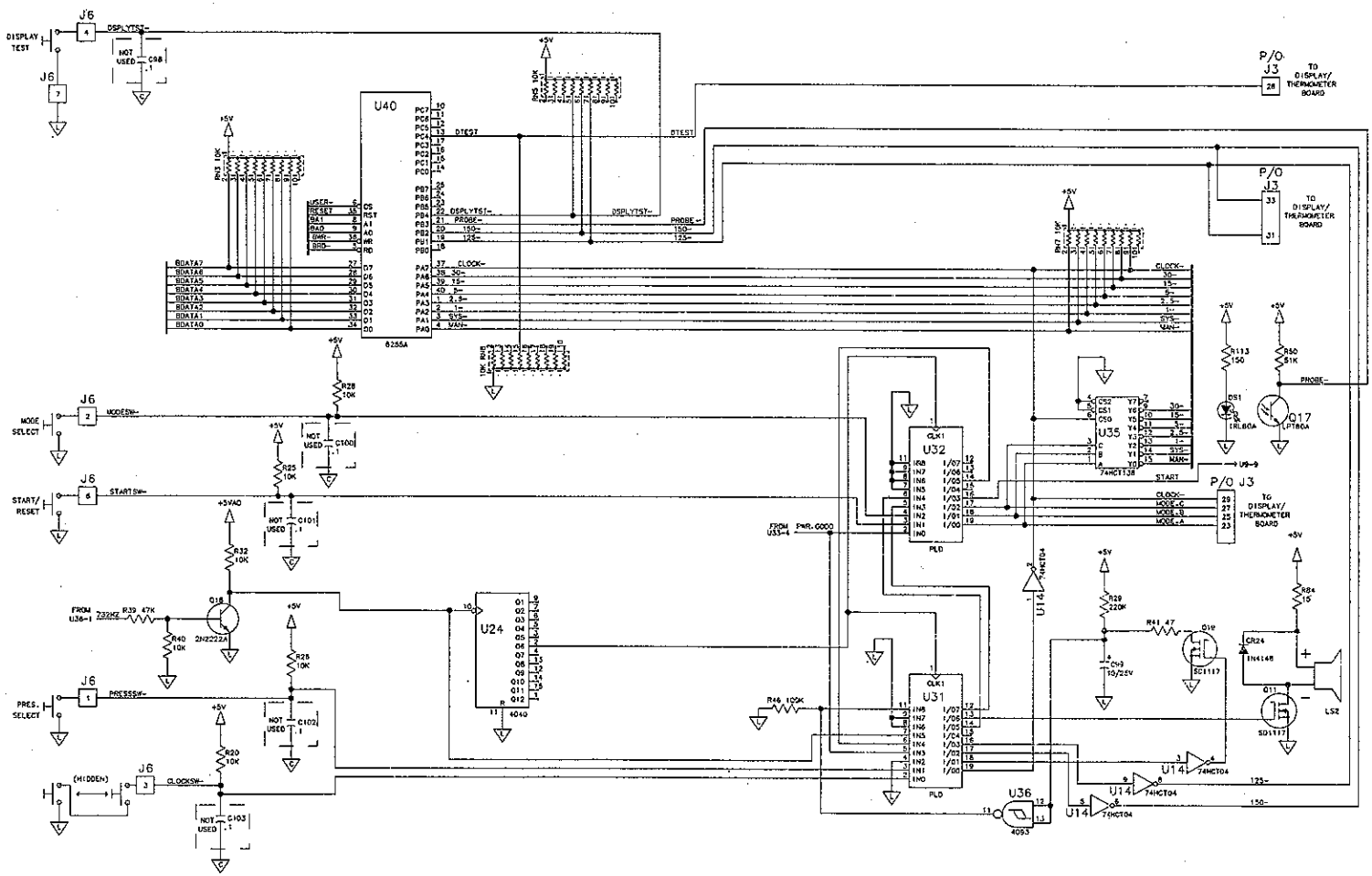

Figure 3-17A. User Interface Logic/Analog Board

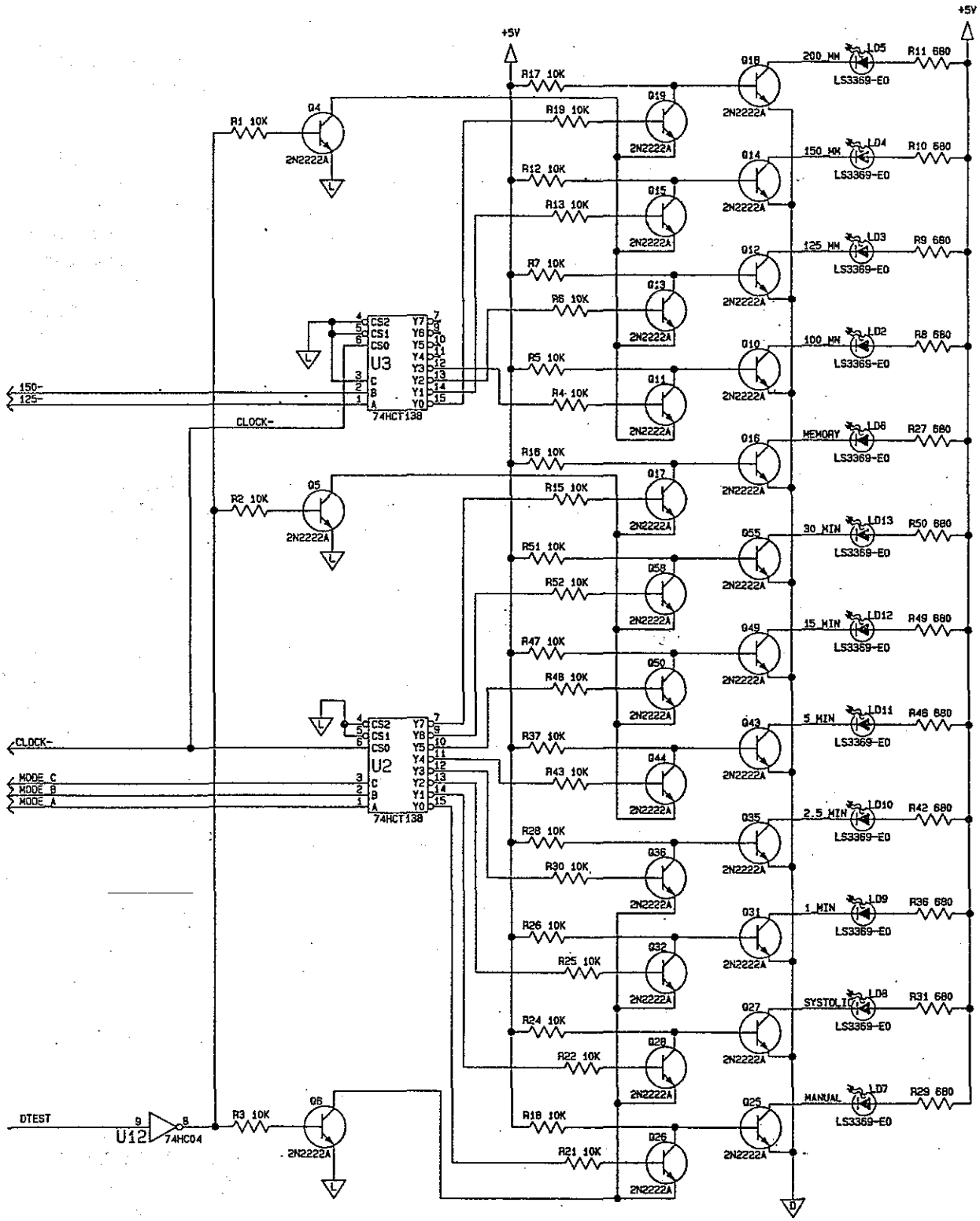

Figure 3-17B. User Interface Display/Thermometer Board

3.6.1 Switches

The mode and pressure select functions and the display test switch are ported through U40. PA0-PA7 and PB0 read the mode function. PB1-PB2 read the pressure function.

A membrane keyboard is used to allow selection of the instrument's operating mode and initial inflation pressure. LED indicators display the selected mode and pressure settings. Two CMOS PLDs (programmable logic device) configured as state machines, and some combinational logic translate the momentary action of the membrane switches to logic levels that emulate multiposition switches. Each mode or pressure keyboard switch actuation advances its respective state machine to the next "switch position." One of four LEDs is illuminated to indicate one of four pressure select options selected, and one of eight LEDs is illuminated to indicate one of eight mode select options selected. Debouncing of the membrane switches is accomplished by the PLD state machines.

To gain access to the real-time clock in CIM equipped instruments, two series connected hidden switches must be actuated simultaneously for a minimum of one second (five seconds maximum) to select the real-time clock mode function.

a. Mode Select

Actuating the MODE SELECT switch increments the PLD mode state machine to the next one of eight mode states. The mode state appears externally at U32 pins 19, 18, and 17 (I/O0, I/O1, and I/O2). (See table 3-4.)

Table 3-4. PLD Mode States

Mode	I/O0	I/O1	I/O2
MEMORY	HI	HI	HI
MANUAL	LO	LO	LO
SYSTOLIC	HI	LO	LO
1 min	LO	HI	LO
2.5 min	HI	HI	LO
5 min	LO	LO	HI
15 min	HI	LO	HI
30 min	LO	HI	HI

There are actually two internal states in the mode select state machine for each external mode state. Each internal state corresponds to a make and then break of the MODE SELECT switch. The real-time clock mode state is an independent state, described below, that externally overrides the mode state.

The MEMORY mode is selected by the software when none of the other seven active-LO modes and the active LO CLK mode are asserted at the input port U40. (Although decoder U35 pin 7 is not connected, it is functionally equivalent to MEMORY-.)

The MANUAL mode has been assigned the state LO LO LO so that it will be selected by default when power is first applied to the PLD, as the output registers are cleared upon initial application of power (i.e., battery installation).

Decoding of the three line mode state to the active-LO linear select method to drive the CPU input port (U40) is accomplished by U35. U2 on the display/thermometer board decodes the mode state to drive the mode indicator LEDs.

Selecting the real-time clock mode does not affect the current state of the mode and pressure select state machines. Selecting the real-time clock mode asserts the signal CLOCK-, which overrides the mode select state at the decoder U35, and blanks the mode and pressure select LEDs by disabling the decoders U2 and U3 on the display/thermometer board. (The signal CLOCK- itself is not actually a clock signal.)

A time delay is provided to avoid inadvertent selection of this function. Actuating the hidden switches turns off Q19, allowing C99 to charge, eventually driving IN8 of PAL U31 LO, selecting the real-time clock function.

Actuation of either the MODE SELECT or PRES. SELECT switch deselects the CLK mode.

b. Pressure Select

Actuating the PRES. SELECT switch increments the PLD pressure state machine to the next one of four pressure states. The pressure state appears externally at U31 pins 17 and 16 (I/02 and I/03) and is inverted by two sections of U14. (See table 3-5.)

Table 3-5. Inverted Pressure States

Pressure	I/02-	I/03-
100 mmHg	HI	HI
125 mmHg	HI	LO
150 mmHg	LO	HI
200 mmHg	LO	LO

There are actually two internal states in the pressure select state machine for each external pressure state. Each internal state corresponds to a make and then break of the PRES. SELECT switch.

The 100 mmHg setting has been assigned the inverted state HI HI so that it will be selected by default when power is first applied to the PLD.

The pressure state is not further decoded, but directly drives the CPU input port U40. U3 on the display/thermometer board decodes the pressure state to drive the pressure indicator LEDs.

c. Audible Feedback

LS2 provides audible feedback for switch actuation. PLD U31 gates a short burst of 732 Hz to LS2 via Q11 upon closure of a MODE SELECT or PRES. SELECT switch, or the hidden switches.

d. Clocks

The PLDs are supplied a 11.44 Hz (87 mSec period) clock divided down by U24 from the 732 Hz clock provided by the processor clock divider U26. This clock is used by the switch debouncing and synchronizing logic in the PLDs. Q18 serves to provide a known logic state for the divider U24 and PLD U31 when the instrument is turned off.

e. Power-Off Mode

The PLDs U31 and U32, and the clock divider U24 remain powered by the +5VAO supply when the instrument is turned off, allowing the pressure and mode settings to be retained.

The PLD inputs are disabled and their outputs are driven to the high impedance state by the PWR_GOOD signal going LO when the instrument is turned off. This disallows mode or pressure selection changes while the instrument is turned off. The PWR_GOOD signal is timed so that it goes LO before the instrument's power supply voltages decay upon instrument "turn off", and goes HI after the power supply voltages have stabilized upon instrument "turn on."

f. Display Test Mode

The pressure indicator and mode indicator LEDs are illuminated via the signal DTEST, along with the rest of the displays during a display test sequence.

g. LED Drivers

The LED drivers are divided into three groups, with the four predrivers in each group controlled by display test control switch Q4, Q5, or Q6, respectively. During normal instrument operation, Q4, Q5, and Q6 are turned on (saturated). This results in all but one of the four predrivers being turned on in the upper group of four (pressure readout) and all but one of the eight predrivers being turned on in the two lower groups of four (mode readout), thus holding off all but one LED driver transistor in each readout.

During the display test function, Q4, Q5, and Q6 are turned off, disabling all twelve predrivers, thus enabling all twelve LED drivers.

U3 decodes the pressure state to one of four active LO levels; turning off one of the four predriver transistors Q11, Q13, Q15, or Q19; enabling one of the four LED drivers Q10, Q12, Q14, or Q18.

U2 decodes the mode state to one of eight active LO levels; turning off one of the eight predriver transistors: Q26, Q28, Q32, Q36, Q44, Q50, Q56, or Q17; enabling one of the eight LED drivers Q25, Q27, Q31, Q35, Q43, Q49, Q55, or Q16.

The thermometer probe detect circuitry (located in the probe storage well) is read at PB3 and is used to detect whether the thermometer probe is in or out of its storage well. A LO signals the CPU to turn on the thermometer and initiate a temperature measurement. This function is described in section 3.10.

The probe detector optics consists of DS1, an IRLED (infrared LED) type IRL-80A, and Q17, a phototransistor type LPT-80A-4. The IRLED is operated in a continuous mode. When a temperature probe is present in the instrument's probe well, the probe body blocks the IR emission traveling from the IRLED to the phototransistor, turning it off (collector is logic HI), thereby causing the thermometer to be turned off by the instrument's CPU. With the probe removed from the well, IR emission from the IRLED (as well as ambient light) reaches the phototransistor, saturating it (collector is logic LO), causing the CPU to turn the thermometer on.

The optics system is enclosed in a light-tight housing, such that ambient light cannot reach the phototransistor when a temperature probe is in place.

Other thermometer function switches are not read by the CPU. The thermometer contains a µcontroller which reads the NORMAL/MONITOR mode switch and the S2 internal DIP switch no. 5 (°F°C) directly.

Other user switches that are not read at U40 include: the START/RESET switch, which is part of CPU RST5.5 (section 3.2.9), and the ON/OFF switch, which is part of an electronic switching circuit on the power regulator board (section 3.9.10).

3.6.2 Speaker Alarm Circuit (figure 3-18)

The port controls the speaker alarm circuit, and is selected by BWR-, BA0 and BA1. BEEP HI (PC0) or BEEP LO (PC1) is issued via U40 to the speaker circuit to generate an audible alarm.

The CPU writes a control word to U40 to issue HI BEEP for a high-pitched (1.46 kHz) audio alarm, or to issue LO BEEP for a low-pitched (732 Hz) audio alarm. Writing another control word will turn the audio alarm off.

The exciter clock frequencies are generated at the clock divider and are gated through U36 by the control signals from U40. FET Q16 pulses the speaker in response to the clock frequencies.

3.6.3 Battery Status Monitor

Battery and A/C status are ported to PB5, 6 and 7.

When operating on battery power, U40 receives signals from the battery status comparator U106 via U104 on the power regulator board. When battery voltage drops below threshold, first LOWBATT- and then DEADBAT- go LO, and these signals are read by the CPU through the user interface port so that the appropriate alarm can be issued.

3.7 DISPLAY FUNCTIONS (figure 3-19)

The display circuit is on the display/thermometer board. The displays are memory mapped to the CPU.

3.7.1 7-Segment Displays (figure 3-20)

a. Systolic and Diastolic

U1 on the display/thermometer board is a self-contained, self-scanning display driver, decoder and display RAM. The display RAM appears as six write-only addresses to the CPU, which correspond to six digits driven by U1. Q3, Q2, Q1, Q9, Q8, and Q7 are the digit drivers, while U1 itself directly provides the segment and decimal point drive.

In operation, one digit at a time is driven. The appropriate lines, SA through SG and SDP, for a given digit are enabled and one of the transistors (Q3, Q2, Q1, Q9, Q8, and Q7), is turned on via a corresponding output, DS1 through DS6, to complete the circuit through the digit being driven. This process is then repeated for the next digit, and this continues at a rate fast enough to make it appear that the six digits are constantly illuminated.

The systolic and diastolic displays are DS1 through DS6 on the display/thermometer board. RN1 determines the current that flows through the display segments. On U1, the D0-D4 inputs are data inputs from the buffered data bus. A1, A2, and A3 are the digit address inputs on the buffered address bus.

b. Pulse

This display operates identically to the systolic and diastolic displays. U4 is the display driver; Q20, Q21, and Q22 being the digit drivers, and RN2 the segment current-limiting resistor. The pulse display is DS7 through DS9 on the display/thermometer board.

3.7.2 Information Display (figure 3-21)

The information display consists of two 4-digit alphanumeric displays, DS15 and DS16 on the display/thermometer board. Each display is a completely self-contained display RAM, decoder, driver and LED display. Each unit appears as 4 write-only addresses to the CPU, and both are enabled (M6-) by address decoder U5-6 on the logic/analog board, along with buffered address bit 2 (BA2). Buffered address bits 0 and 1 (BA0, BA1) select the individual character position, and buffered data bits 0 through 6 (BDATA0 through BDATA6) contain the character data.

3.7.3 Temperature Display

The temperature display (5-digit LEDs) is driven from drivers located on the display/thermometer board, and is covered in more detail in section 3.10.

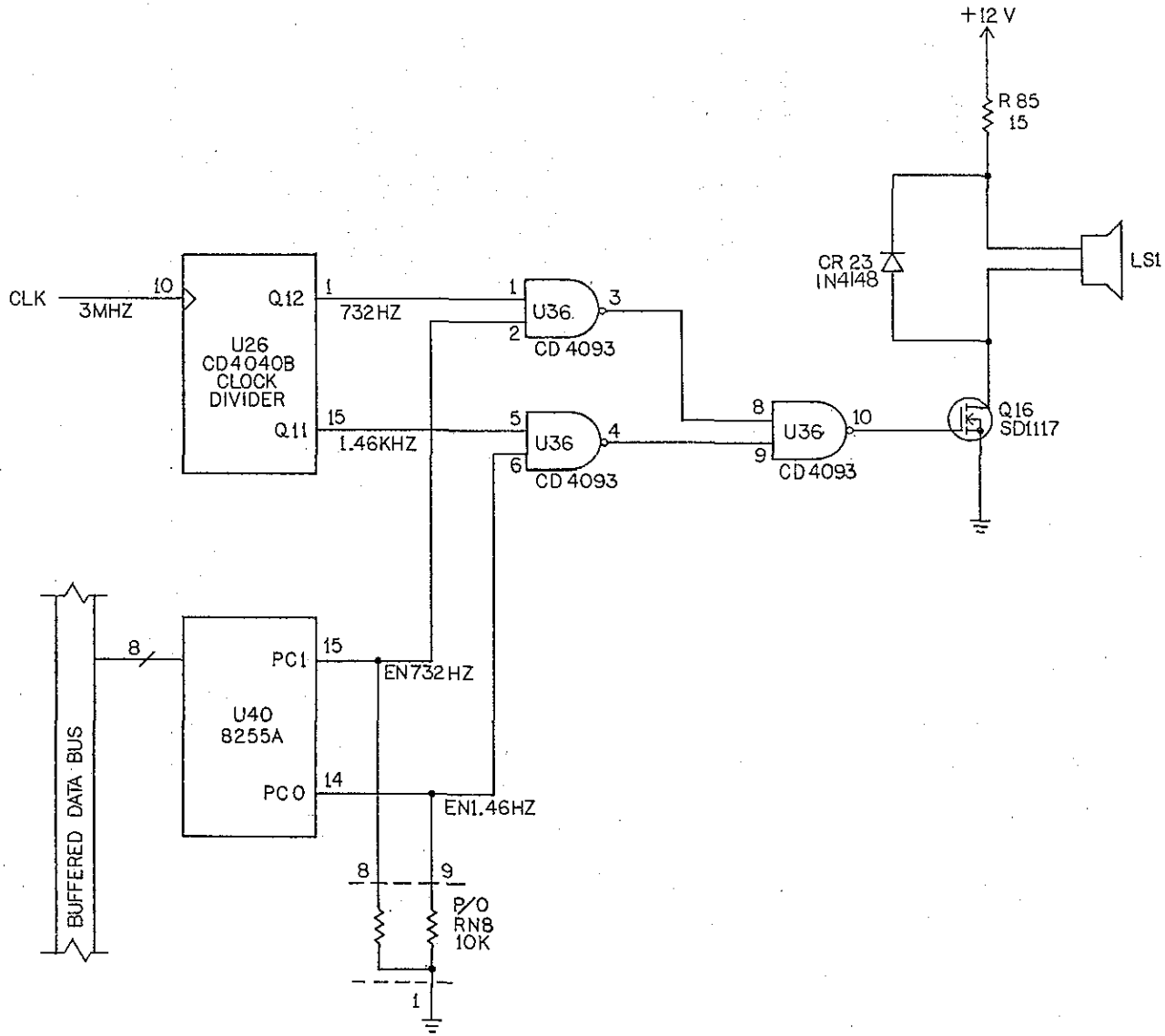

Figure 3-18. Speaker Alarm Circuit

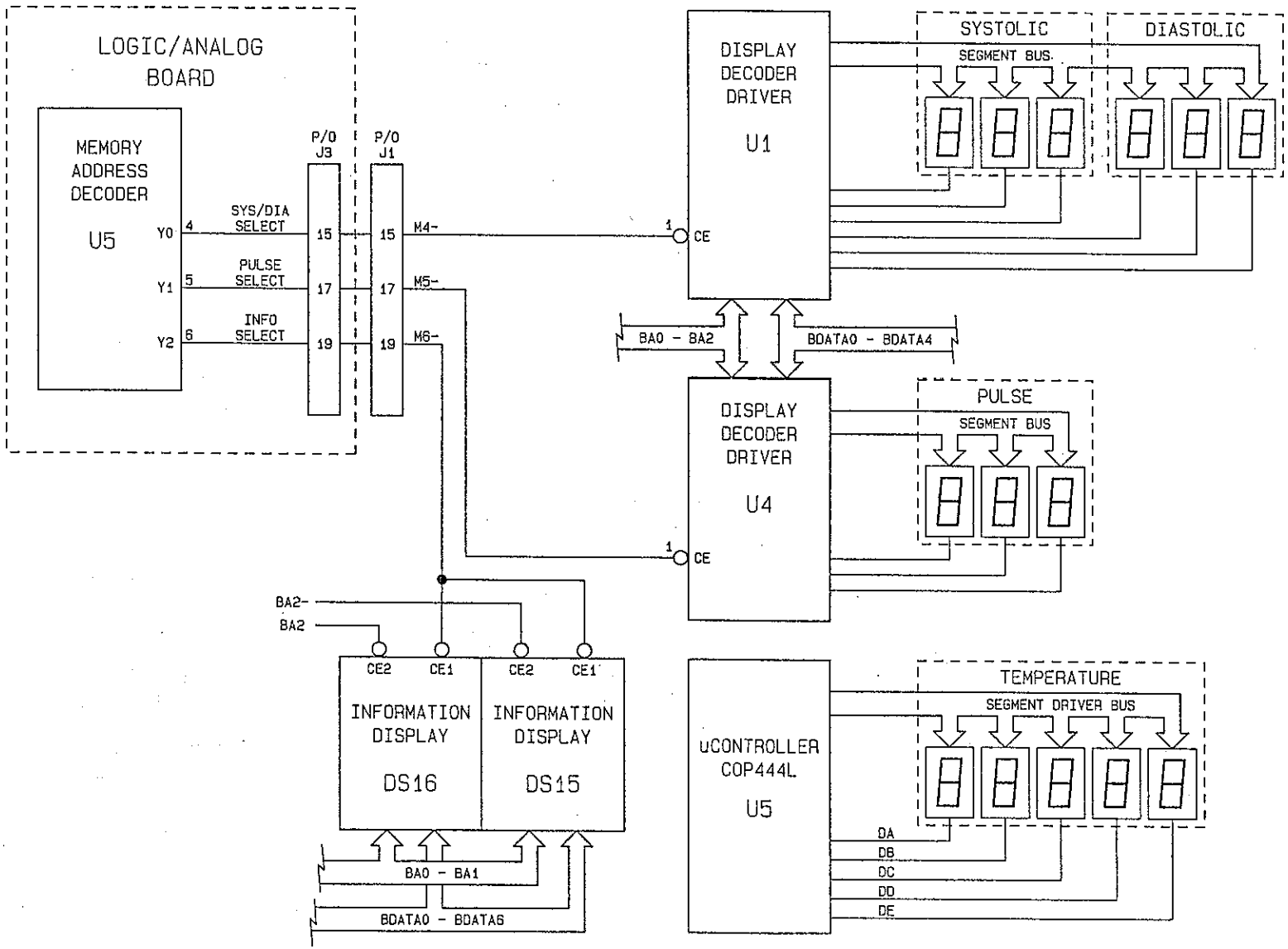

Figure 3-19. Display and Display Driver Boards Block Diagram

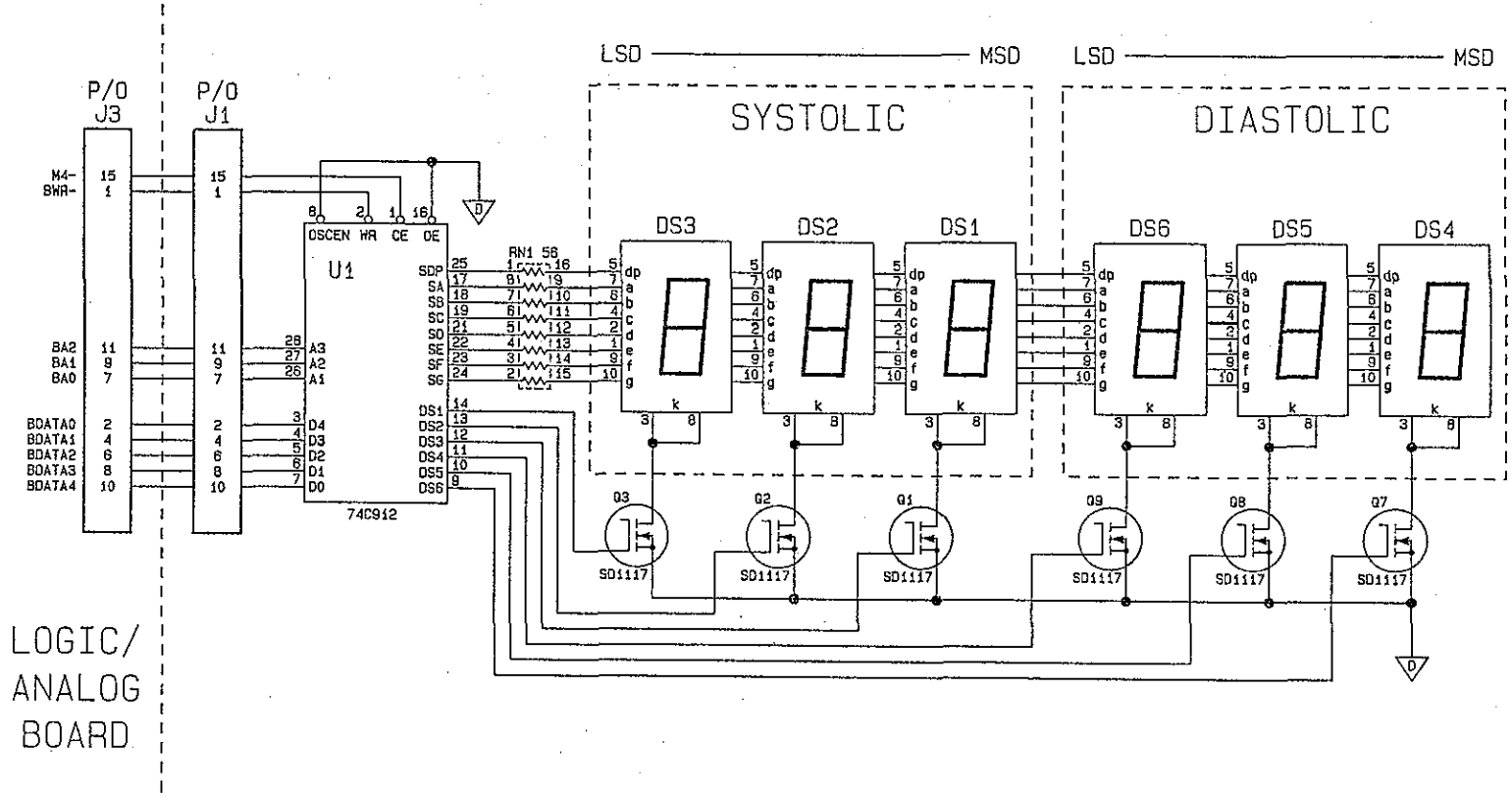

Figure 3-20. 7-Segment Display Driver Circuit

3.8 HARDWARE FAILSAFE CIRCUIT (figure 3-22A, 3-22B)

The purpose of the hardware failsafe circuitry is to protect the individual whose blood pressure is being taken from an overpressure or excessive inflation time condition if the CPU has lost control of the pneumatic system. The failsafe is tested by the CPU at instrument start-up, and then write-locked from the CPU so that it is independent and can only be monitored.

a. Disable Flip-Flop

U25-13 is the disable flip-flop. At instrument start-up, it is cleared via U23-3 and the time constant of R8 and C67 delaying the application of logic HI to U23 pin 1. This causes pin 3 to be momentarily HI, clearing U25-13. U25 pin 13 (Q) will be LO and pin 12 ($\overline{Q}$) will be HI, turning on Q2, which turns on Q3 via R17. Q3 collector provides power (FS+5) to the leaker, enables part of the dump valve driver and enables part of the pump driver (power regulator board). If U25-1 becomes set for any reason, power is removed from the leaker driver, opening the leaker valve; the dump valve driver is disabled, opening the dump valve; and the pump driver is disabled so that the pump will not operate.

Q12 on the logic/analog board is the dump valve disable. Q115 on the power regulator board is the pump disable. It is normally always turned on via Q117. Normally, Q117 is turned on via R155 by FS+5. The state of the failsafe flip-flop is monitored via Q2, Q3, Q117, Q115 and U104-12 (FSDIS).

b. Clock Chain

The clock chain is a series of binary ripple counters used to derive the various timing signals in the failsafe. A 375 kHz clock from the system clock divider drives U8 and gate U19-3. U8 is a 12-stage ripple counter which divides the 375 kHz clock down to 91.6 Hz at pin 1 (Q12), which then drives gate U19-10. U19-3 can be enabled to provide the 375 kHz clock to U6-6 by the CPU setting line FS4 high to quickly test the 4.5 minute timer, or the 91.6 Hz clock can be provided to U6-6 by the CPU setting line FS3 low, enabling U19-10 via inverter U19-4. The 91.6 Hz clock is selected by default as U7 is reset at power-on or as the failsafe is write-locked after the power-on test.

U6-6 provides the 91.6 Hz (or 375 kHz) clock to another ripple counter, U17. Assuming normal operation using the 91.6 Hz clock, U17 pin 12 (Q1) provides a 45.8 hz clock to the 4.5 minute timer and a 1.43 hz clock (700 milliseconds) to U25-3 and U25-11. If the failsafe flip-flop (U25-13) is set, U17 is held reset via U3-10 and U3-4 to prevent the failsafe from clocking itself back out of a fault condition.

c. Clock Loss Watchdog

The clock loss watchdog detects the loss of the operating clock from the failsafe circuitry. In normal operation, the clock signal, which appears at U6 pin 6, is coupled through C42 to Q4. This keeps Q4 turning on and off, which in turn, keeps C41 discharged. Thus, U23 pins 8 and 9 are high and pin 10 is LO. If the clock fails, Q4 will no longer conduct, allowing C41 to charge through R22 toward logic LO. When U23 pins 8 and 9 reach LO, pin 10 is driven HI, directly setting U25-13.

d. 4.5 Minute Timer

The 4.5 minute timer is a backup to the software inflation timer. It is enabled when the cuff pressure exceeds 20 mmHg and held reset when the cuff pressure is less than 20 mmHg. The pressure signal appears at comparator U38-3 input via multiplexer U27 and divider R43 and R34. R24, R31, and R35 form a divider which furnishes the references level for comparator U38-1 (and U38-7, the overpressure sense comparator). When the cuff pressure exceeds 20 mmHg, U38 pin 1 goes HI, pulling the inverter U19 pins 12 and 13 high via R45. U19 pin 11 then goes LO, removing the reset from the 14 stage ripple counter U22. U22 will then count the 45.8 Hz clock from U17. If the cuff pressure drops below 20 mmHg within 4.5 minutes of exceeding 20 mmHg, U38 pin 1 will go LO, causing U19 pin 11 to go HI, and hold U22 reset. If the cuff pressure does not drop below 20 mmHg, U22 will continue to count; 4.5 minutes after counting has started, pins 2 (Q13) and 3 (Q14) will both be HI, allowing the AND gate U6 pin 8 to go HI. U13 pin 10 will then go LO. The action that U25-1 and U25-13 then take will be described in step e of this section. U38 pin 1 is monitored by the CPU via the input port U18 (FSCOMP) pin 6.

e. Overpressure Detection

The failsafe overpressure detection is a backup to the software overpressure protection. It is implemented with a comparator monitoring the pressure channel that has a threshold of 335 mmHg. The pressure signal appears at comparator U38 pins 3 and 6 input via multiplexer U27 and divider R43 and R34. R24, R31, and R35 form a divider which furnishes the reference levels of 1.99V at U38-5 and 0.118V at U38-2. If the pressure rises above about 335 mmHg, U38 pin 7 will go LO, causing inverter U3 pin 11 to go HI, and U13 pin 10 to go LO. This removes the reset from U25-4 and allows the next clock from U17 pin 4 to clock U25 pin 1 (Q) HI. The following clock, 700 milliseconds later, will clock U25 pin 13 (Q) HI, disabling

the instrument. U17 will be held reset via U3-10 and U3-4, removing the clock from U25, so that the state of U25 cannot be changed. If the overpressure is a transient and falls back below 335 mmHg before the next 700 millisecond clock clocks U25-11, U25-4 will be reset (pin 1 LO) and no fault will be detected. The mechanical overpressure sensing switch (on the pneumatic module) is connected to U38 pin 7 via J7 on the logic/analog board, and J1 and J4 on the transition board. It is normally open. If the cuff pressure exceeds the switch's threshold, it closes, connecting U38 pin 7 to ground with the same effect as if comparator U38-7 detected a pressure greater than 335 mmHg. The mechanical overpressure switch is a backup to the overpressure comparator in the event the pressure voltage fails to appear at the overpressure comparator.

f. Power-On Testing

When the instrument is first turned on, the failsafe is exercised to simulate faults and test the comparators (U38-1 and U38-7). Extra circuitry is included for power-on testing.

When the instrument is turned on, a power-on reset is obtained from the time constant of R8 and C67 which is shaped by Schmidt triggers U23-3 and U23-4. The reset pulse from U23-3 clears flip-flop U25-13 and initializes counter U17 to zero via U3-10 and U3-4. The reset pulse from U23-4 clears RS flip-flop U13-6 and U13-9 so that U13 pin 9 is LO and clears output port U7 via U3-3 so that all six outputs Q1 through Q6 are LO. The 91.6 Hz clock is now selected via FS3 (U7 pin 10) and the multiplexer U27 is set to the pressure signal via FS0 and FS1 (both low), U27 pins 10 and 9, respectively. This is the normal operating mode of the failsafe except that now the CPU can write to U7 and change the state of any of the signals FS0 through FS5. The CPU can now exercise the failsafe. Signals FS0 and FS1 select simulated pressures of less than 20 mmHg (U27 pin 5), greater than 20 mmHg but less than 335 mmHg (U27 pin 2) or greater than 335 mmHg (U27 pin 4) to test the comparators U38-1 and U38-7. The simulated pressures are obtained from a divider consisting of R37, R19, R23, and R30.

Signal FS2 (U7 pin 7) is used to clear U25-13 via U39-12 and U23-3 after a simulated fault. Signal FS4 (U7 pin 12), when HI, selects the 375 kHz clock to rapidly test the failsafe system. Signal FS3 (U7 pin 10), when LO, selects the 91.6 Hz clock for normal operation. By setting FS3 low and FS4 high, the clock can be removed entirely to test the clock loss detector Q4 and U23-10 and associated components.

Signal FS5 (U7 pin 15) is used to write-lock the failsafe system output port U7. When the CPU has completed the power-on failsafe testing, it writes a high to FS5. This sets R/S flip-flop U13-6 and U13-9, making U13 pin 9 high. U3 pin 3 is then low, holding U7 in a reset condition so that the CPU cannot write to it. This isolates the failsafe from the CPU so that a CPU failure cannot render the failsafe ineffective. In the event that the CPU cannot complete the failsafe testing and write-lock the output port, there is a circuit to automatically write-lock in about six seconds. This circuit is implemented with RC network R7 and C77. When C77 charges through R7 to the low threshold of U23-11, U23 pin 11 goes high, setting R/S flip-flop U13-6 and U13-9 in the same manner as FS5 would have.

3.9 POWER REGULATOR BOARD FUNCTIONS (figure 3-23)

Incoming AC power is stepped down by a transformer. It is then rectified, filtered and regulated to provide a +14 VDC voltage source. This voltage source charges the battery pack and is further regulated to provide +5 VDC and -12 VDC. An on/off flip-flop is used to turn the +12 VDC, +5 VDC, and -12 VDC on and off for the rest of the instrument. A battery voltage sensing circuit is used to signal the CPU when a low or discharged battery voltage condition exists.

3.9.1 Transformer, Rectifier, and Filter (figure 3-24 and 3-25)

Figure 3-24 represents the AC power input circuits. The ground terminal is connected to the instrument ground. The instrument is protected by a 1 amp circuit breaker. The line voltage is stepped down to 20 VAC nominal by transformer T1. A snubber network consisting of C1 and R1 on the primary of T1 absorbs transients on the AC line.

Referring to figure 3-25, diodes CR101 through CR104 and filter capacitor C102 rectify and filter the voltage from the secondary of T1 to an unregulated voltage of nominally 28 VDC.

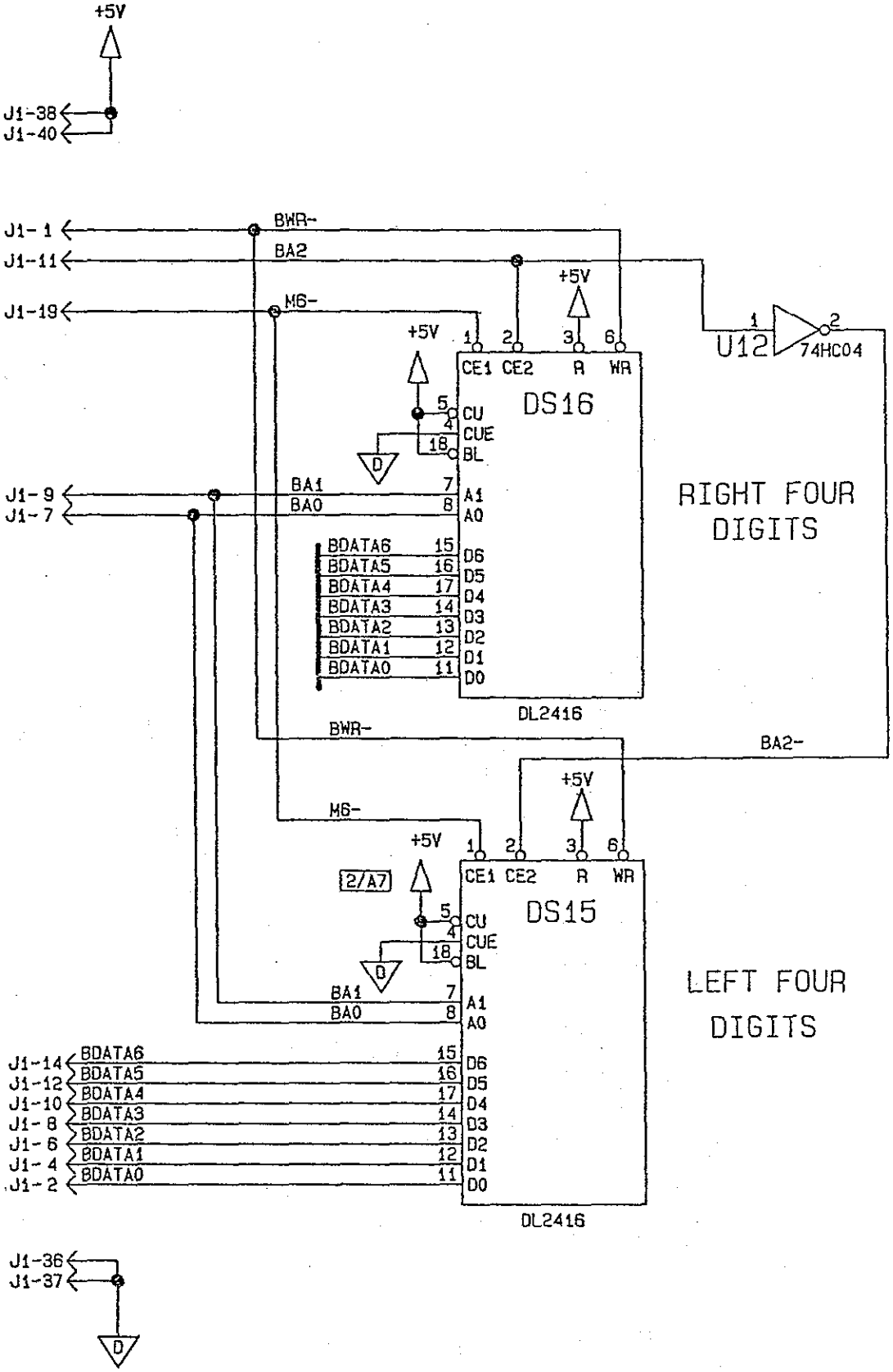

Figure 3-21. Information Display Driver Circuit

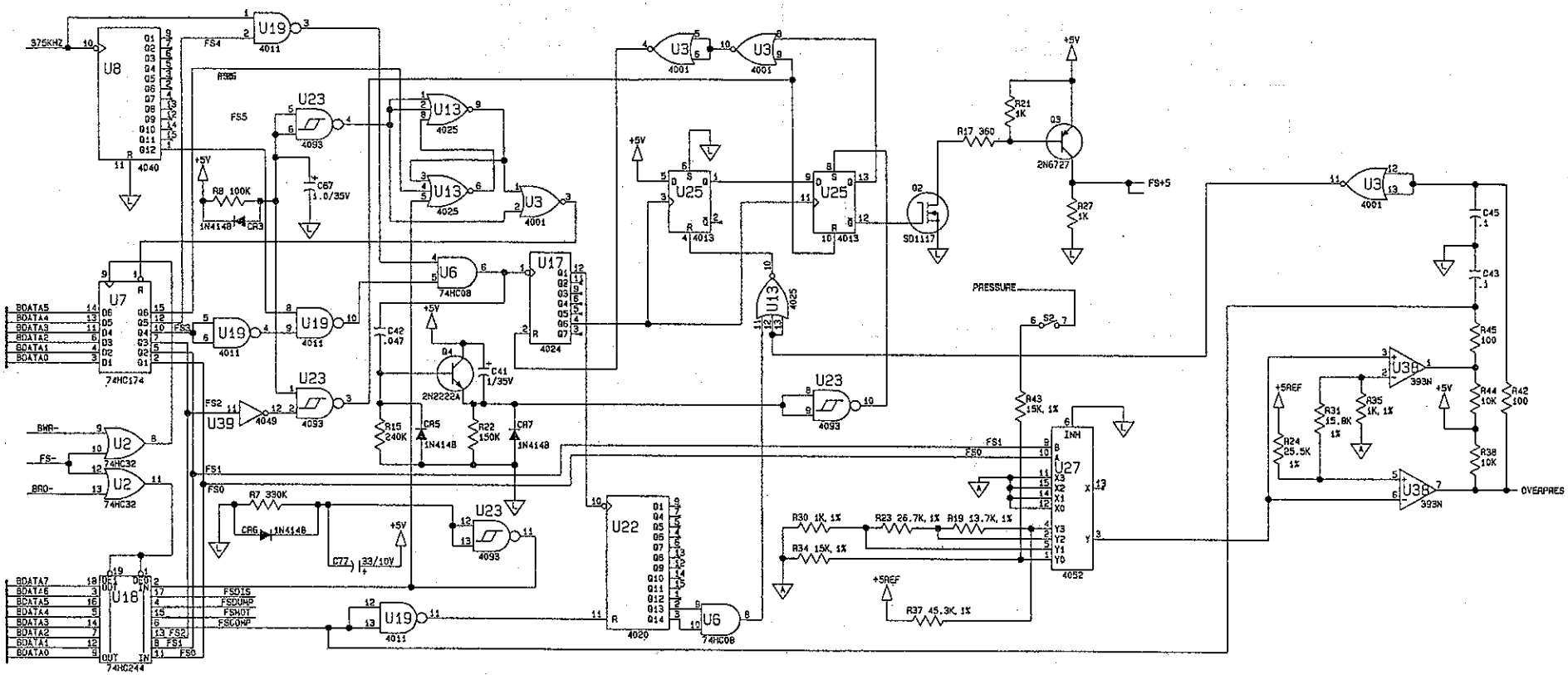

Figure 3-22A. Failsafe Circuit